DOCKET NO. 93-C-091D1 (STMI01-00012) **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	:	Pervez H. Sagarwala et al
Prior Serial No.	:	08/885,636
Filed	:	Herewith
For	:	CMOS INTEGRATED CIRCUIT DEVICE WITH LDD N-CHANNEL TRANSISTOR AND NON-LDD P-CHANNEL TRANSISTOR
Prior Group No.	:	2822
Prior Examiner	:	M. Trinh

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D. C. 20231

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KATHY LONGENECKER
(Printed or typed name of person signing the certificate)

Kathy Longenecker
(Signature of the person signing the certificate)

Sir:

PRELIMINARY AMENDMENT

Prior to examination, please amend the above-identified divisional application as follows:

IN THE SPECIFICATION

1. Please insert the following statement on page 1 of the specification:

"This application is a division of prior U.S. Application Serial No. 08/885,636 filed on June 30, 1997."

IN THE CLAIMS

Please cancel claims 8-26 without prejudice. Please amend the remaining claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

1. (amended) A CMOS integrated circuit device comprising:

a plurality of p-channel transistors formed in active surface areas of n-type regions, wherein the p-channel transistors do not have LDD source/drain regions;

a plurality of n-channel transistors formed in isolated active surface areas of p-type regions;

gate electrodes for the p-channel and n-channel transistors, the gate electrodes overlying and being insulated from the respective active surface areas, wherein the gate electrodes for the p-channel transistors have a width less than a minimum channel length required for the p-channel transistors;

p-type source and drain regions for the p-channel transistors, each p-type source and drain region consisting of a low resistivity region;

n-type source and drain regions for the n-channel transistors, each n-type source and drain region having a low resistivity region and an LDD region;

each gate electrode having a pair of sidewall spacers each having an inner and an outer portion, wherein the inner portions of the sidewall spacers for each p-channel transistor gate

electrode has a width which, taken on each side of the respective gate electrode for the respective p-channel transistor and combined with the width of the respective gate electrode for the respective p-channel transistor, exceeds a minimum channel length for the respective p-channel transistor;

each p-channel low resistivity region located under the outer portion and at least a part of the inner portion of its respective sidewall spacer;

each n-channel low resistivity region located under at least a part of the outer portion and a part of the inner portion of its respective sidewall spacer; and

each n-channel LDD region extending from its respective low resistivity region to underlie the inner portion of its respective sidewall spacer.

2. (unchanged) The integrated circuit of claim 1, wherein the inner portion of the sidewall spacer comprises an oxide.

3. (unchanged) The integrated circuit of claim 1, wherein the inner portion of the sidewall spacer comprises an oxide.

4. (unchanged) The integrated circuit of claim 1, wherein the p-channel source and drain comprise silicon implanted wtih BF_2.

5. (amended) The integrated circuit of claim 1, wherein:

the distance between low resistivity regions of the source and drain regions of the p-channel transistor is between the p-channel minimum length and the p-channel maximum length, wherein:

the p-channel minimum length is a distance below which the transistor will not operate reliably due to short channel effects; and

the p-channel maximum length is a distance above which the transistor will not turn on efficiently.

6. (amended) The integrated circuit of claim 1, wherein:

the distance between the low resistivity regions of the n-channel transistor is between the n-channel minimum LDD length and the n-channel maximum LDD length, wherein:

the n-channel minimum LDD length is a distance below which the transistor will not operate reliably due to short channel effects; and

the n-channel maximum LDD length is a distance above which the transistor will not turn on efficiently.

7. (unchanged) The integrated circuit of claim 1, wherein the sidewall spacers have a total width of approximately 500 to 2500 Å.

Please add the following new claims:

--27. (newly added) A CMOS integrated circuit structure, comprising:

an n-channel transistor including lightly doped source and drain regions within a p-type region of a substrate; and

a p-channel transistor without lightly doped source and drain regions within an n-type region of the substrate, the p-channel transistor including:

a gate electrode having a width less than a channel length of a channel for the p-channel transistor; and

first sidewall spacers adjacent opposing sides of the gate electrode and overlying at least a portion of the channel for the p-channel transistor.

28. (newly added) The CMOS integrated circuit structure of claim 27, wherein the width of the gate electrode is less than the minimum channel length required for the p-channel transistor.

29. (newly added) The CMOS integrated circuit structure of claim 28, wherein the first sidewall spacers have a width which, taken on opposing sides of the gate electrode and combined with the width of the gate electrode, exceeds the minimum channel length required for the p-channel transistor.

30. (newly added) The CMOS integrated circuit structure of claim 29, wherein the width of the first sidewall spacers, taken on opposing sides of the gate electrode and combined with the width of the gate electrode, exceeds the minimum channel length required for the p-channel transistor plus a diffusion distance for implanted dopants forming source and drain regions for the p-channel transistor.

31. (newly added) The CMOS integrated circuit structure of claim 30, further comprising:

second sidewall spacers adjacent the first sidewall spacers and overlying source and drain regions for the p-channel transistor.

32. (newly added) The CMOS integrated circuit structure of claim 30, wherein the n-channel transistor further comprises:

a gate electrode having a width approximately equal to a minimum channel length required for the n-channel transistor; and

sidewall spacers adjacent to opposing sides of the n-channel transistor gate electrode and overlying the lightly doped source and drain regions.

33. (newly added) An intermediate structure for use in forming a CMOS integrated circuit, comprising:

a p-type region for an n-channel transistor including lightly doped source and drain regions;

an n-type region for a p-channel transistor without lightly doped source and drain regions;

a gate electrode overlying a portion of the n-type region, the gate electrode having a width less than a minimum channel length required for the p-channel transistor; and

an insulating layer over a top and sides of the gate electrode, the insulating layer having a thickness which, taken on opposing sides of the gate electrode and combined with the width of the gate electrode, exceeds the minimum channel length required for the p-channel transistor.

34. (newly added) The intermediate structure of claim 33, wherein the insulating layer forms a mask for implanting source and drain regions for the p-channel transistor.

35. (newly added) The intermediate structure of claim 34, wherein the insulating layer has a thickness which, taken on opposing sides of the gate electrode and combined with the width of the gate electrode, exceeds the minimum channel length required for the p-channel transistor plus a diffusion distance for implanted dopants forming the source and drain regions for the p-channel transistor.

36. (newly added) The intermediate structure of claim 35, further comprising:

source and drain regions for the p-channel transistor within the n-type region, wherein edges of the source and drain regions are spaced apart from the sides of the gate electrode.

37. (newly added) The intermediate structure of claim 36, wherein the source and drain regions are low resistivity regions.

38. (newly added) The intermediate structure of claim 33, further comprising:

second insulating layer overlying the first insulating layer to form sidewall spacers adjacent the gate electrode upon etching of the insulating layer and the second insulating layer.

39. (newly added) The intermediate structure of claim 33, further comprising:

a n-channel transistor gate electrode overlying a portion of the p-type region;

lightly doped source and drain regions within the p-type region aligned with the n-channel transistor gate electrode.--

REMARKS

Claims 1-7 and 27-39 are pending in the present application.

Claim 1 was amended to conform to the claims in the parent application; claims 5-6 were amended to correct typographical errors.

Claims 27-39 were added.

Examination of the application on the merits is respectfully requested.

AMENDMENTS WITH MARKINGS TO SHOW CHANGES MADE

Claims 1 and 5-6 were amended herein as follows:

1. (amended) A CMOS integrated circuit device comprising:

a plurality of p-channel transistors formed in active surface areas of n-type regions, wherein the p-channel transistors do not have LDD source/drain regions;

a plurality of n-channel transistors formed in isolated active surface areas of p-type regions;

gate electrodes for the p-channel and n-channel transistors, the gate electrodes overlying and being insulated from the respective active surface areas, wherein the gate electrodes for the p-channel transistors have a width less than a minimum channel length required for the p-channel transistors;

p-type source and drain regions for the p-channel transistors, each p-type source and drain region consisting of a low resistivity region;

n-type source and drain regions for the n-channel transistors, each n-type source and drain region having a low resistivity region and an LDD region;

each gate electrode having a pair of sidewall spacers each having an inner and an outer portion, [each sidewall spacer corresponding to an underlying source and drain region]wherein

the inner portions of the sidewall spacers for each p-channel transistor gate electrode has a width which, taken on each side of the respective gate electrode for the respective p-channel transistor and combined with the width of the respective gate electrode for the respective p-channel transistor, exceeds a minimum channel length for the respective p-channel transistor;

each p-channel low resistivity region located under the outer portion and at least a part of the inner portion of its respective sidewall spacer;

each n-channel low resistivity region located under at least a part of the outer portion and a part of the inner portion of its respective sidewall spacer; and

each n-channel LDD region extending from its respective low resistivity region to underlie the inner portion of its respective sidewall spacer.

5. (amended) The integrated circuit of claim 1, wherein:

the distance between low resistivity regions of the source and drain regions of the p-channel transistor is between the p-channel minimum length and the p-channel maximum length, wherein:

the p-channel minimum length is a distance below which the transistor will not operate reliably due to short channel effects; and

the p-channel maximum length is a distance [the] above which the transistor will not turn on efficiently.

6. (amended) The integrated circuit of claim 1, wherein:

the distance between the low resistivity regions of the n-channel transistor is between the n-channel minimum LDD length and the n-channel maximum LDD length, wherein:

the n-channel minimum LDD length is a distance below which the transistor will not operate reliably due to short channel effects; and

the n-channel maximum LDD length is a distance above which the transistor will not turn on efficiently.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***dvenglarik@novakov.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

NOVAKOV DAVIS & MUNCK, P.C.

Date: February 28, 2001

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